AMENDMENTS TO THE CLAIMS

No claim is amended. A complete listing of the claims is provided as follows:

1. (Original) A circuit design simulator, comprising:

a stored electronic representation of a circuit design, said circuit design including at least one interface between a digital circuit and an analog circuit, said interface comprising a node at which said digital circuit provides an output and at which said analog circuit receives an input and provides a conditional output, said output taking on any one of several states including a digital high state, digital low state, or a high impedance state; and

at least one processor for simulating operation of said circuit design, said at least one processor dynamically determining whether or not to apply each conditional output to its respective node according to the state of the digital circuit output connected to the node.

2. (Original) The circuit design simulator of claim 1, wherein said at least one processor applies a conditional output to its respective node when the digital circuit output connected to the node is not in said high impedance state, and otherwise does not apply said conditional output to its respective node.

3. (Original) A method for simulating electronic activity at a digital/analog interface in a circuit design, said method comprising the steps of:

identifying an interface between a digital circuit and an analog circuit, said interface comprising a node at which said digital circuit provides an output and at which said analog

circuit receives an input, said output taking on any one of several states including a digital high state, digital low state, or a high impedance state;

modeling said output as a digital output signal from said digital circuit to said node when said output is not in said high impedance state, and as an analog output signal from said analog circuit to said node when said output is in said high impedance state; and

dynamically switching between said digital output signal and said analog output signal based upon whether or not said output is in said high impedance state.

4. (Original) The method of claim 3, wherein attributes of said analog output signal are solved for while assuming that no current flows from said digital circuit to said node when said output is in said high impedance state.

5. (Original) A method for simulating electronic activity at a digital/analog interface in a circuit design, said method comprising the steps of:

identifying an interface between one or more digital circuits and an analog circuit, said interface comprising a node at which each of said one or more digital circuits provides an output and at which said analog circuit receives an input, each said output taking on any one of several states including a digital high state, digital low state, or a high impedance state;

modeling each said output as a digital output signal from the corresponding digital circuit to said node when the output is not in said high impedance state, and as an analog output signal from said analog circuit to said node when each said output is in said high impedance state; and

dynamically switching between said digital output signal and said analog output signal based upon whether or not each of said outputs is in said high impedance state.

6. (Original) The method of claim 5, wherein attributes of said analog output signal are solved for while assuming that no current flows from said one or more digital circuits to said node when each of said outputs is in said high impedance state.

7. (Original) The method of claim 5, wherein each said output from said one or more digital circuits are connected to a bus contention element, said method further comprising the step of collectively resolving each said output from said one or more digital circuits into a single output signal, said single output signal taking on any one of several states including said digital high state, said digital low state, or said high impedance state.

8. (Original) A method for simulating electrical operation at a digital/analog interface in a circuit design, said method comprising the steps of:

identifying an interface between a digital circuit and an analog circuit, said interface comprising a node at which said digital circuit either outputs a digital signal or else presents a high impedance output so as to be effectively isolated from the node, and at which said analog circuit receives an input signal at an input port;

adding a conditional output signal from the input port of said analog circuit to said node; and

simulating electrical operation at said interface by applying said conditional output signal to said node when said digital circuit presents a high impedance output, and applying said digital signal to said node otherwise.

9. (Original) A computer-readable medium on which is embodied a set of programmed instructions that cause one or more processors to perform a sequence of steps, said steps comprising:

identifying an interface between one or more digital circuits and an analog circuit, said interface comprising a node at which each of said one or more digital circuits provides an output and at which said analog circuit receives an input, each said output taking on any one of several states including a digital high state, digital low state, or a high impedance state; and

modeling each said output as a digital output signal from the corresponding digital circuit to said node when the output is not in said high impedance state, and as an analog output signal from said analog circuit to said node when each said output is in said high impedance state.

10. (Original) The computer-readable medium of claim 9, wherein said programming instructions further cause said one or more processors to perform the step of dynamically switching between said digital output signal and said analog output signal based upon whether or not each of said outputs is in said high impedance state.

11. (Original) The computer-readable medium of claim 10, wherein said programming instructions further cause said one or more processors to solve for attributes of said analog output signal while assuming that no current flows from said one or more digital circuits to said node when each of said outputs is in said high impedance state.

12. (Original) The computer-readable medium of claim 10, wherein each said output from said one or more digital circuits are connected to a bus contention element, said programming instructions causing said one or more processors to further perform the step of collectively resolving each said output from said one or more digital circuits into a single output signal, said single output signal taking on any one of several states including said digital high state, said digital low state, or said high impedance state.

13. (Original) A method for simulating a circuit design, comprising the steps of:

identifying interfaces between one or more digital circuit outputs and an analog circuit input, wherein each of said one or more digital circuit outputs can present a high impedance state;

modeling one or more of said interfaces by adding an output from an analog circuit receiving said analog circuit input to the interface; and

simulating electrical operation at each modeled interface by resolving an electrical state of the interface using only the output from the analog circuit when all of the one or more digital circuit outputs are in a high impedance state, and resolving the electrical state of the interface using the one or more digital circuit outputs otherwise.

14. (Original) A mixed analog/digital simulator comprising:

a simulation processor; and

said simulation processor including a computer-readable medium on which is embodied a set of programmed instructions that cause said simulation processor to simulate the operation of a design circuit, wherein said design circuit includes:

(1) a digital circuit, said digital circuit having an output;

(2) a network electrically coupled to said output of said digital circuit, said network formed by electrically coupling an input of each of a plurality of circuit blocks at a network input node;

(3) said circuit blocks including at least one analog circuit, said analog circuit having an analog circuit input electrically coupled to said network input node;

(4) said analog circuit having an input mode of operation for receiving an input signal at said analog circuit input and an output mode of operation for producing an output signal at said analog circuit input;

(5) said output of said digital circuit being applied to said network input node when said digital circuit is in a non-high-impedance state; and

(6) said output signal of said analog circuit being applied to said network input node when said digital circuit is in a high-impedance state.

15. (Original) The simulator of claim 14 in which said output signal of said analog circuit is operably coupled to a plurality of digital circuit outputs using a bus.

16. (Original) The simulator of claim 14 wherein said input mode and output mode are selected automatically and dynamically according to the state of said digital circuit.

17. (Original) A method of simulating mixed analog/digital systems, comprising:

transforming an input of an analog circuit into an ioput, said ioput having a conditional output feeding back to a bus, said ioput being operable under a high-impedance input state, and said ioput capable of accepting a digital signal input and producing an analog signal output;

electrically coupling said ioput to a digital circuit output and to inputs of a plurality of additional circuits;

receiving said digital signal input at said ioput when said digital circuit output is in a non-high-impedance state; and

applying said analog signal output at said ioput when said digital circuit output is in a high-impedance state.

18. (Original) The method of claim 17 in which said step of electrically coupling comprises coupling said ioput to a plurality of digital circuit outputs using a bus.

CONCLUSION

On the basis of the above, reconsideration and allowance of the claims is believed to be warranted and such action is respectfully requested. If the Examiner has any questions or comments, the Examiner is respectfully requested to contact the undersigned at the number listed below.

Respectfully submitted,

Bingham McCutchen LLP

Dated: October 28, 2004

By: _____
Stuart J. West
Reg. No. 43,258

Three Embarcadero Center, Suite 1800
San Francisco, CA 94111-4067
Telephone: (650) 849-4930
Facsimile: (650) 849-4800